OLLSCOIL NA hÉIREANN, GAILLIM H
NATIONAL UNIVERSITY OF IRELAND, GALWAY

SEMESTER II EXAMINATIONS 2001/2002

THIRD YEAR ELECTRONIC ENGINEERING
THIRD YEAR ELECTRONIC AND COMPUTER ENGINEERING

EE321 ANALOGUE SYSTEMS DESIGN II

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Duration of Examination: **TWO** hours
Instructions: Answer **THREE** questions

1.

(a) Write a description for any four of the following types of diode: **[4 x 3 marks]**

- Germanium diode
- Schottky diode
- Varactor diode
- LED
- Flyback diode
- Photo diode

(b) (i) What type of circuit is shown in Fig. 1? **[1 mark]**

(ii) Explain the two modes of operation. **[2 marks]**

(iii) For a sinusoidal input waveform V_s with a peak-to-peak voltage of 7.5 V, sketch the output waveform V_o. **[2 marks]**

(iv) What is the average DC value of V_o? **[1 mark]**

(v) How would V_o change if the ideal diodes were replaced with real diodes? **[2 marks]**

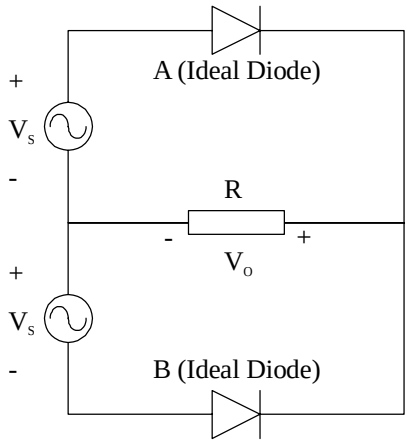

Fig. 1

[cont'd]

2.

(a) (i) Draw a simple model for a real diode. **[1 mark]**

(ii) Sketch the characteristic for a real diode. **[2 marks]**

(iii) What are the main differences between a regular diode and a Zener diode? **[3 marks]**

(iv) Sketch the characteristic for a Zener showing the various regions of operation. **[3 marks]**

(b) A Zener diode circuit for voltage regulation is given in Fig. 2.

(i) In which region does the Zener diode operate for the voltage regulator application? **[1 mark]**

(ii) For varying source voltage and load current, analyse the circuit to determine the proper range of values for R_i that will allow the Zener to maintain a constant output voltage. **[6 marks]**

(iii) Explain why upper and lower limits must be placed on the value of R_i. **[2 marks]**

(iv) Define percentage regulation for the Zener diode voltage regulator. **[2 marks]**

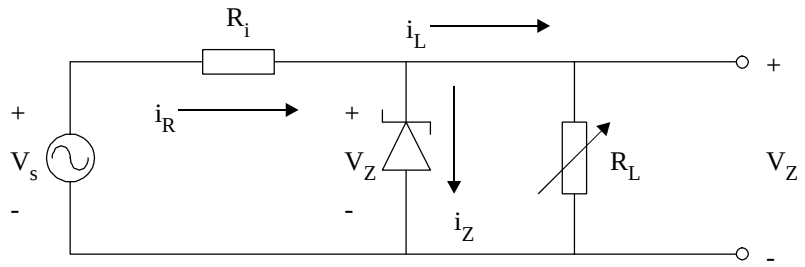

Fig. 2

3.

(a) Perform a DC analysis of the base biasing section of the common emitter amplifier as shown in Fig. 3, and hence derive formulæ for the position of the DC operating point. **[8 marks]**

(b) Explain why it is important as regards small signal voltage amplification to set the quiescent point in the BJT's linear mode of operation using the DC bias circuit. **[4 marks]**

(c) What is the effect of the bypass capacitor in this circuit? **[1 mark]**

(d) Draw a small signal model for the common emitter amplifer circuit in Fig. 3, and using this model derive an expression for the gain of the amplifier. **[7 marks]**

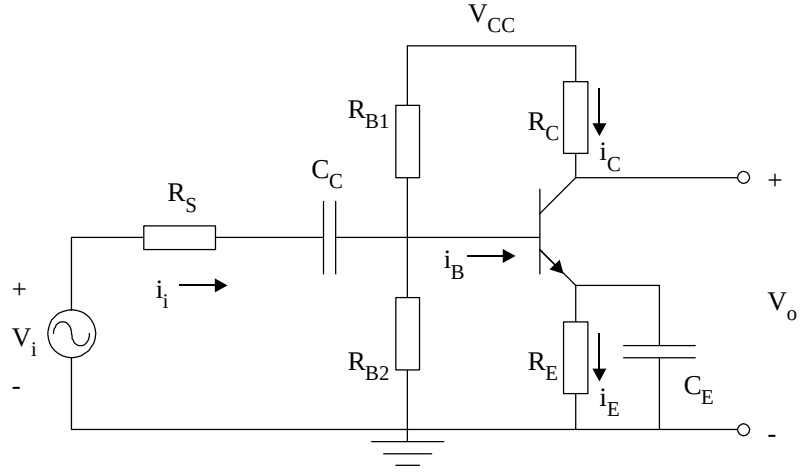

Fig. 3

[cont'd]

4.

(a) Illustrate the n-channel JFET device operation modes using cross sectional diagrams. **[6 marks]**

(b) Calculate the DC operating point of the JFET amplifier shown in Fig. 4, where I_{DSS} = 8 mA and V_{DSPO} = 6 V. **[9 marks]**

$$I_{DSPO} = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GSCO}}\right)^2$$

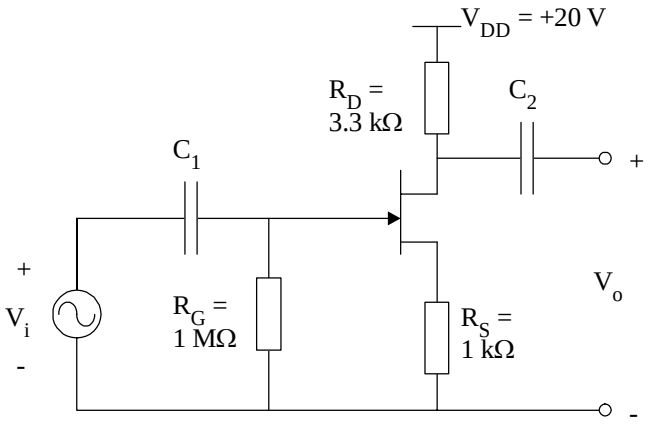

Fig. 4

(c) Illustrate the D-MOSFET and explain how the conducting channel can be "enhanced" by a correctly applied gate voltage. **[5 marks]**

5.

(a) Explain the following points with respect to the Schmitt Trigger circuit of Fig. 5:

(i) Circuit operation **[4 marks]**
(ii) Derivation of trip points **[4 marks]**
(iii) Hysteresis characteristics **[4 marks]**

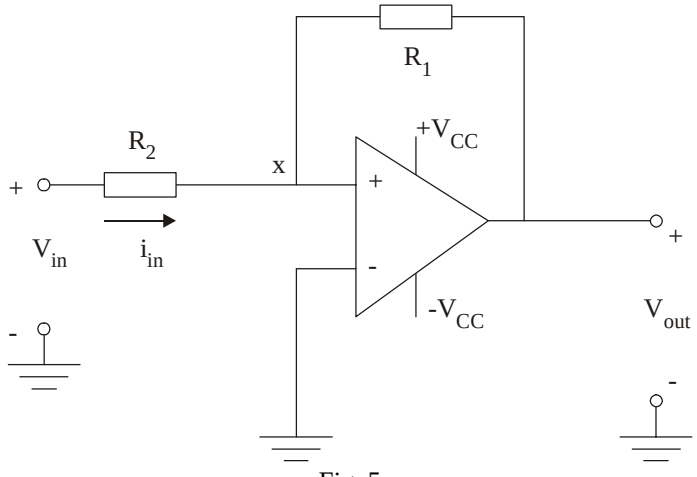

Fig. 5

(b) Explain briefly what is meant by the following specifications in practical operational amplifier circuits (suggest typical values where appropriate):

(i) Input offset current **[2 marks]**
(ii) Input offset voltage **[2 marks]**
(iii) Slew rate **[2 marks]**
(iv) CMRR **[2 marks]**